

*Fig. 1*

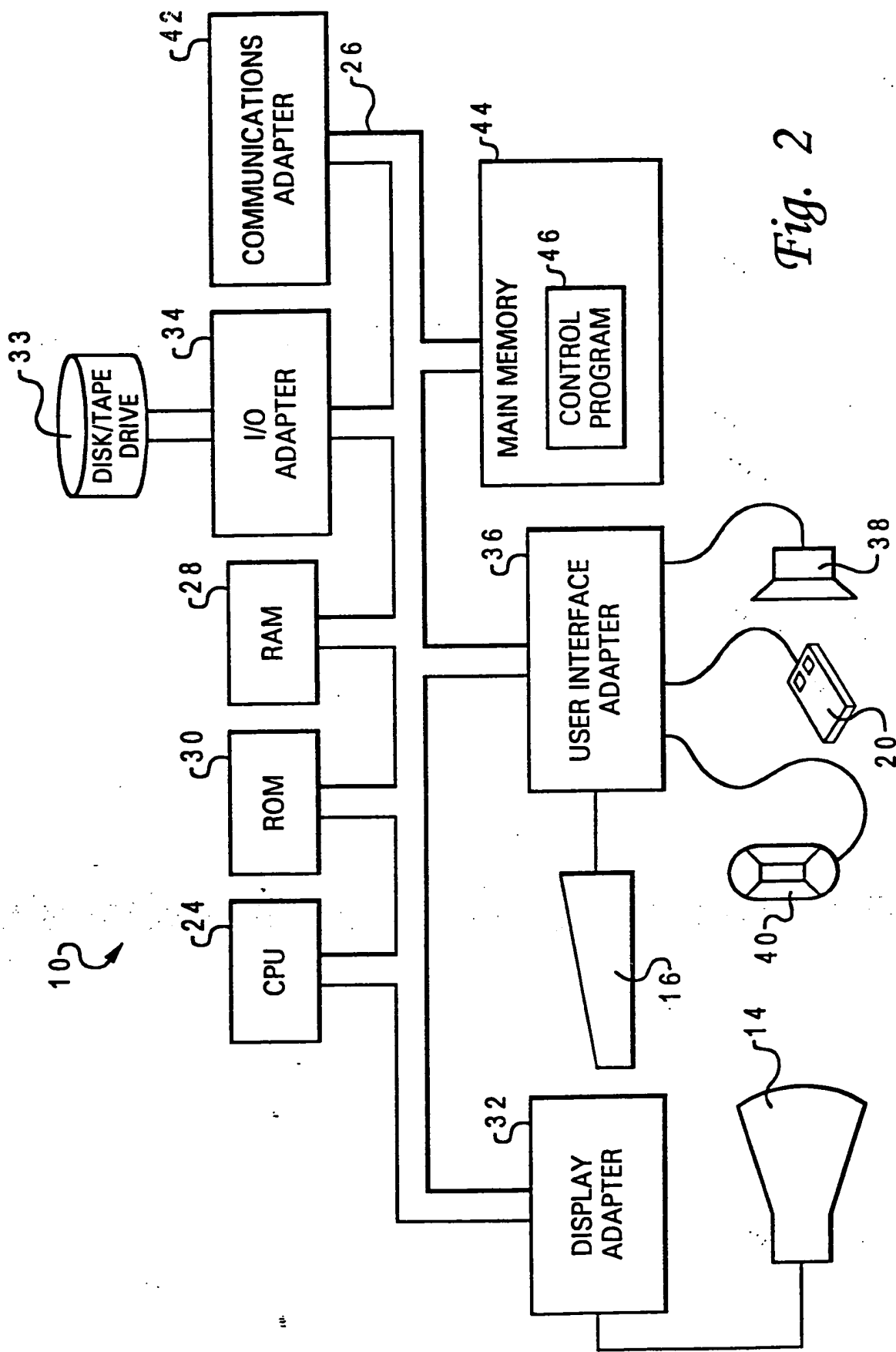


Fig. 2

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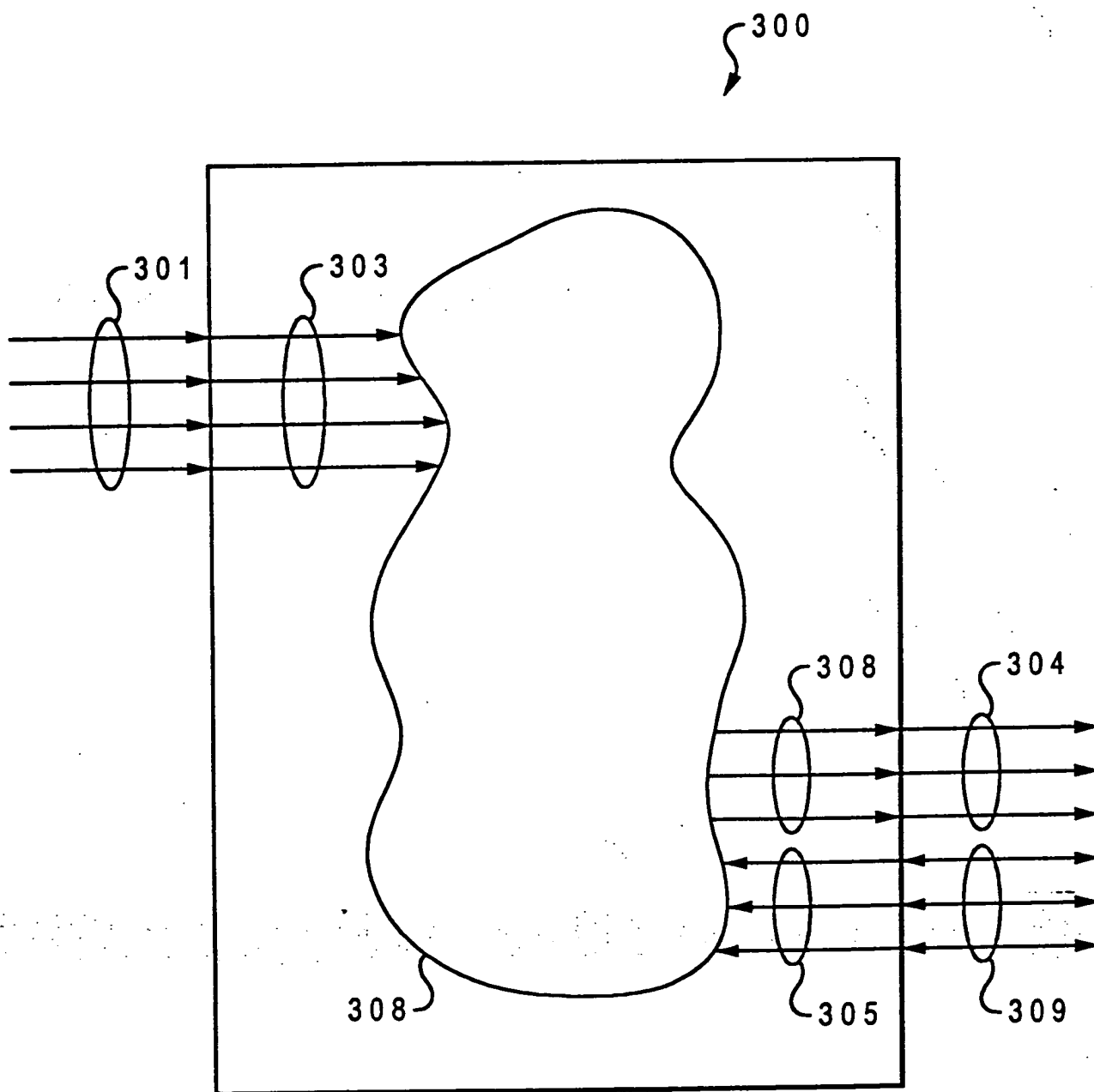


Fig. 3A

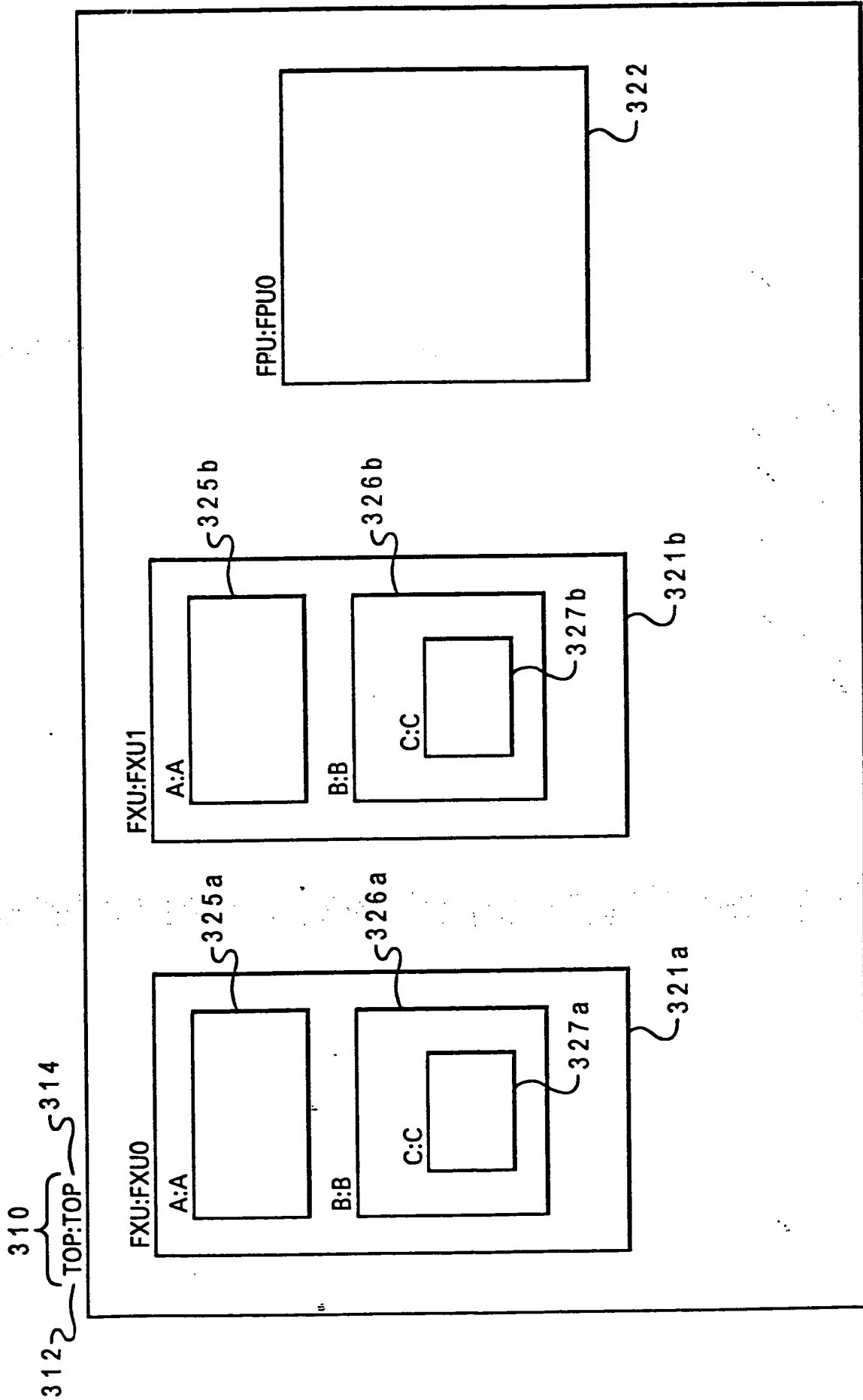
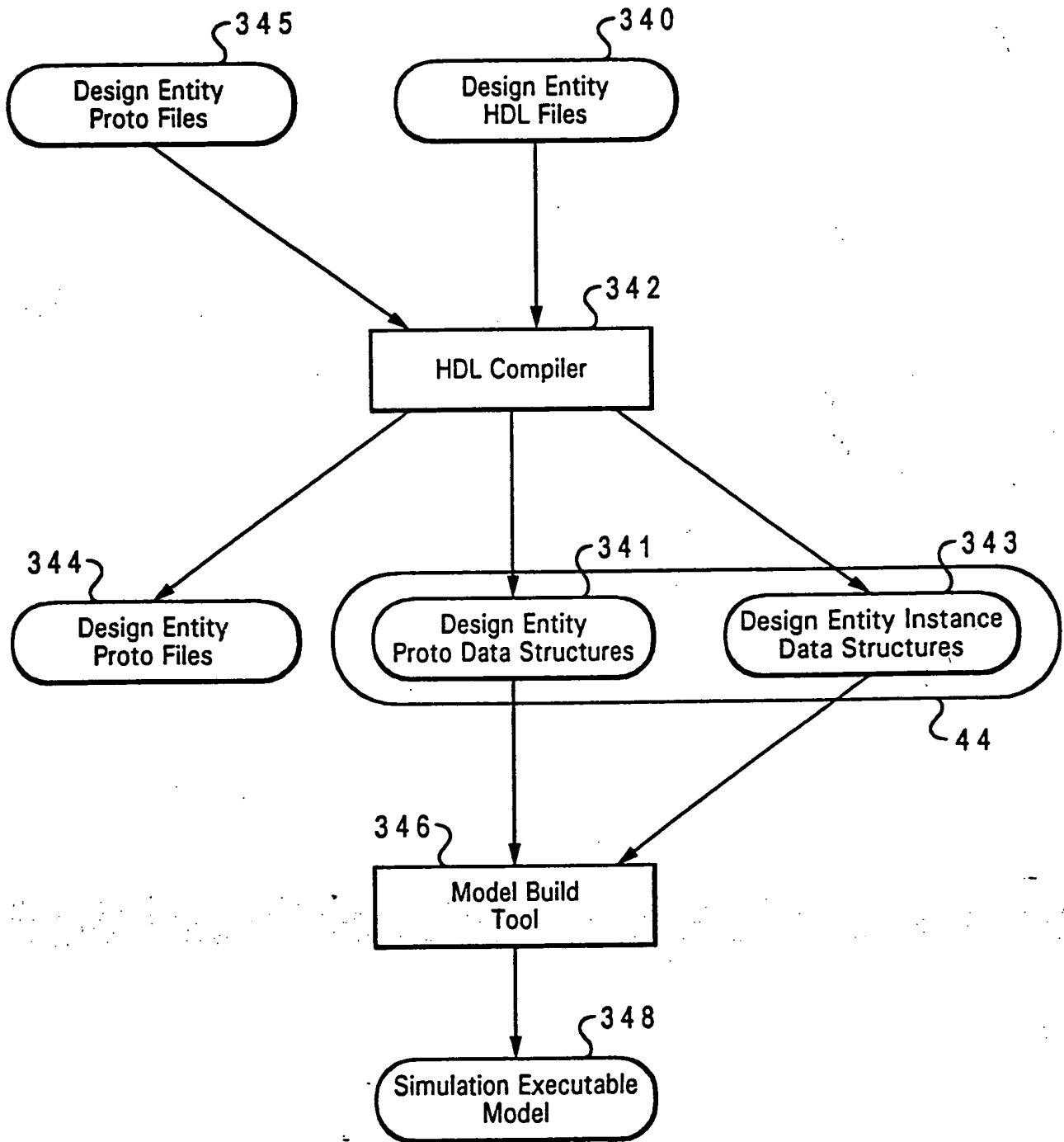


Fig. 3B



*Fig. 3C*

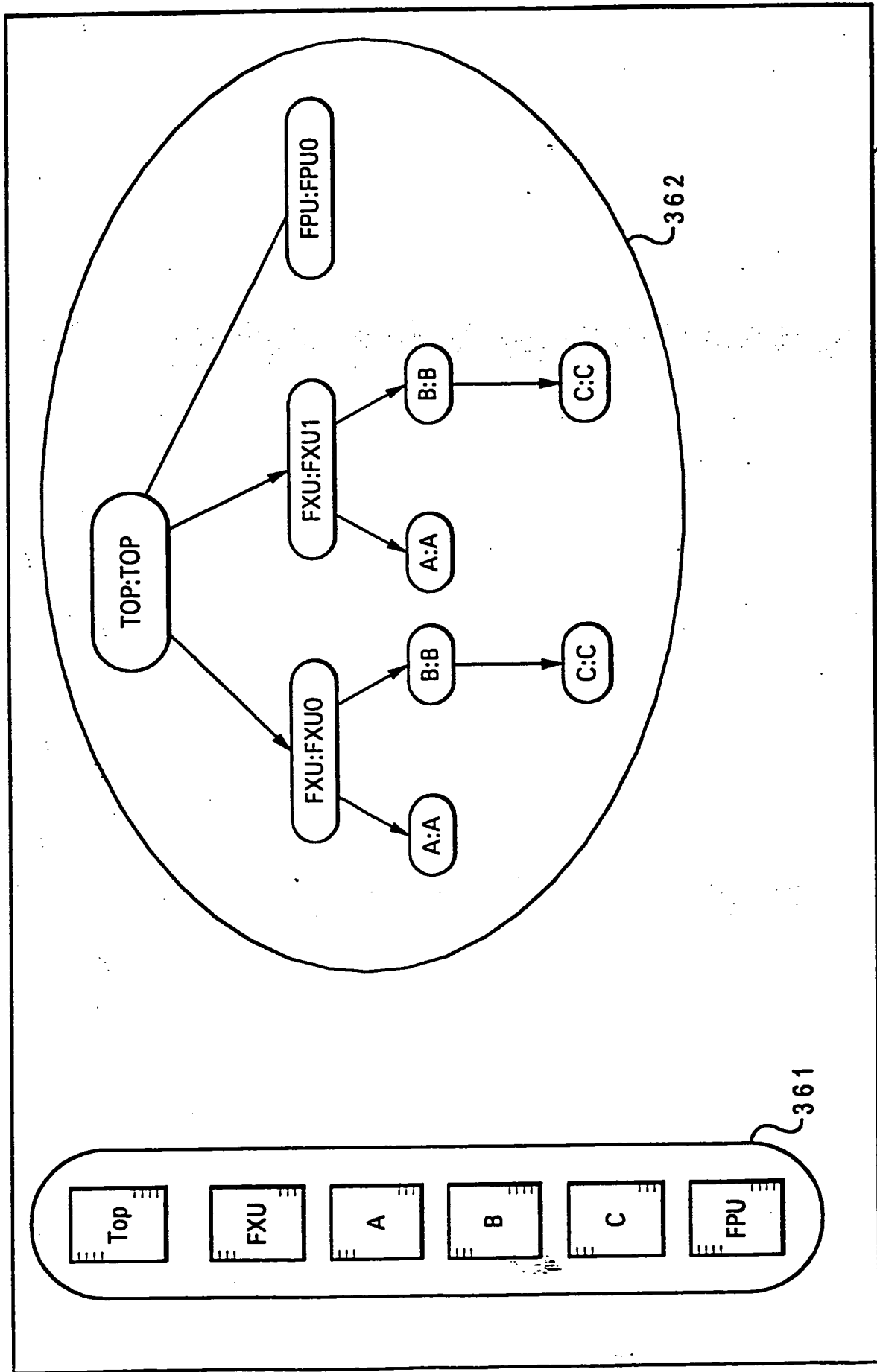


Fig. 3D

006237 60875250

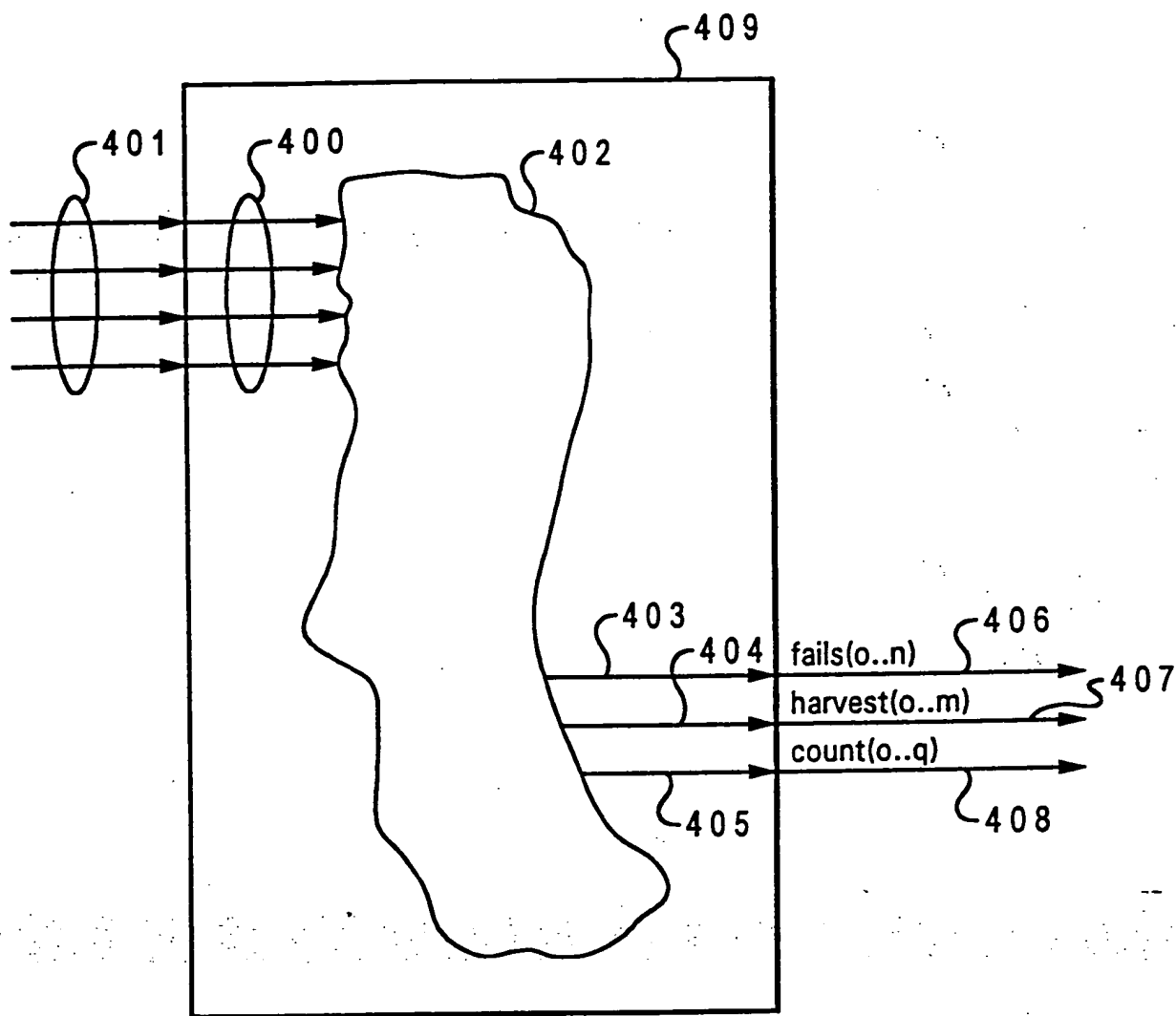


Fig. 4A

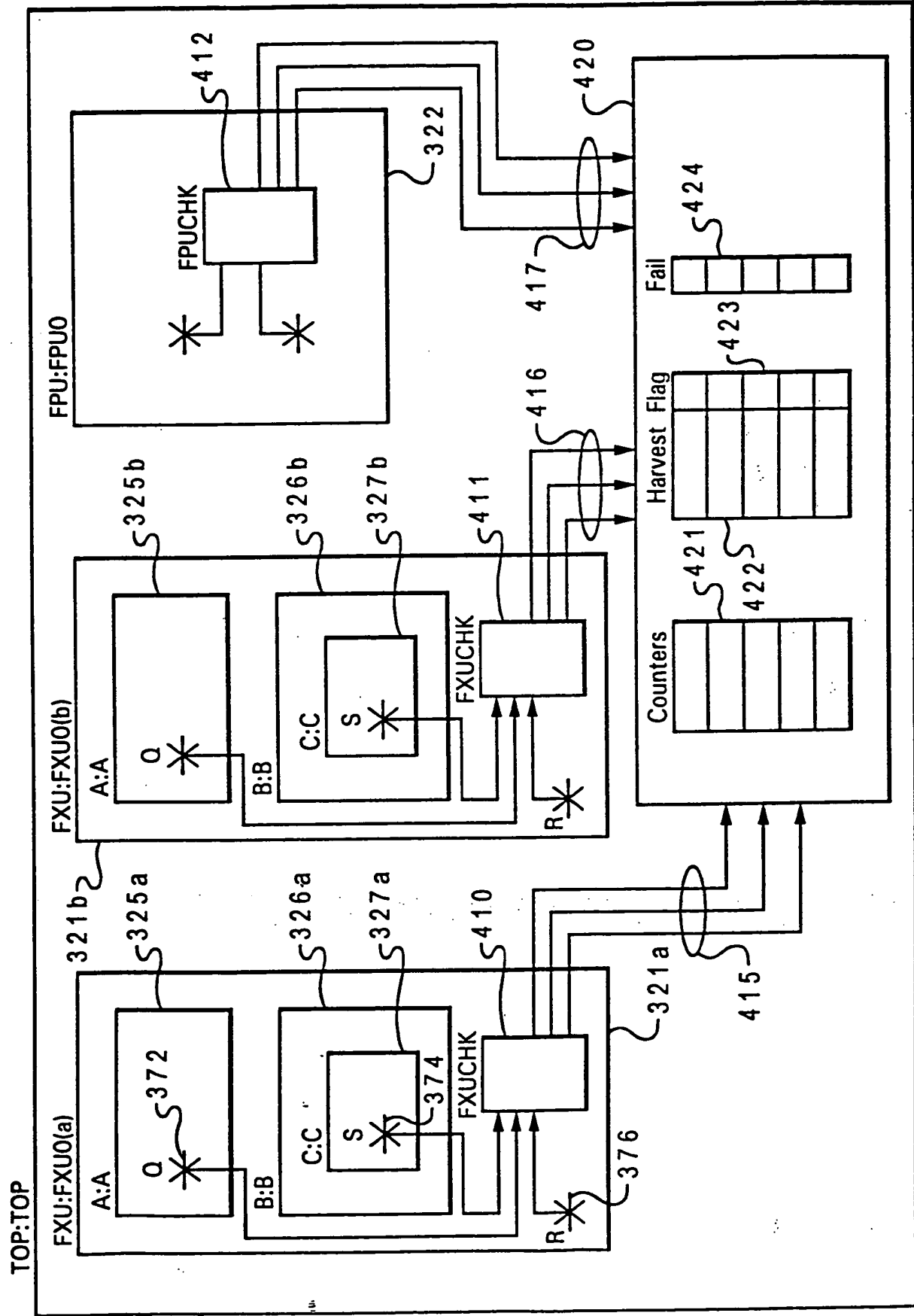


Fig. 4B



# ENTITY FXUCHK IS

```

PORT(  S_IN      :  IN std_ulogic;
        Q_IN      :  IN std_ulogic;
        R_IN      :  IN std_ulogic;
        clock      :  IN std_ulogic;
        fails      :  OUT std_ulogic_vector(0 to 1);
        counts     :  OUT std_ulogic_vector(0 to 2);
        harvests   :  OUT std_ulogic_vector(0 to 1);
);

```

4 5 0

4 5 2 { --!! BEGIN  
--!! Design Entity: FXU;

4 5 3 { --!! Inputs  
--!! S\_IN => B.C.S;  
--!! Q\_IN => A.Q;  
--!! R\_IN => R;  
--!! CLOCK => clock;  
--!! End Inputs

4 5 4 { --!! Fail Outputs;  
--!! 0 : "Fail message for failure event 0";  
--!! 1 : "Fail message for failure event 1";  
--!! End Fail Outputs;

4 5 5 { --!! Count Outputs;  
--!! 0 : <event0> clock;  
--!! 1 : <event1> clock;  
--!! 2 : <event2> clock;  
--!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;  
--!! 0 : "Message for harvest event 0";  
--!! 1 : "Message for harvest event 1";  
--!! End Harvest Outputs;

4 5 7 { --!! End;

4 5 1

4 4 0

## ARCHITECTURE example of FXUCHK IS

BEGIN

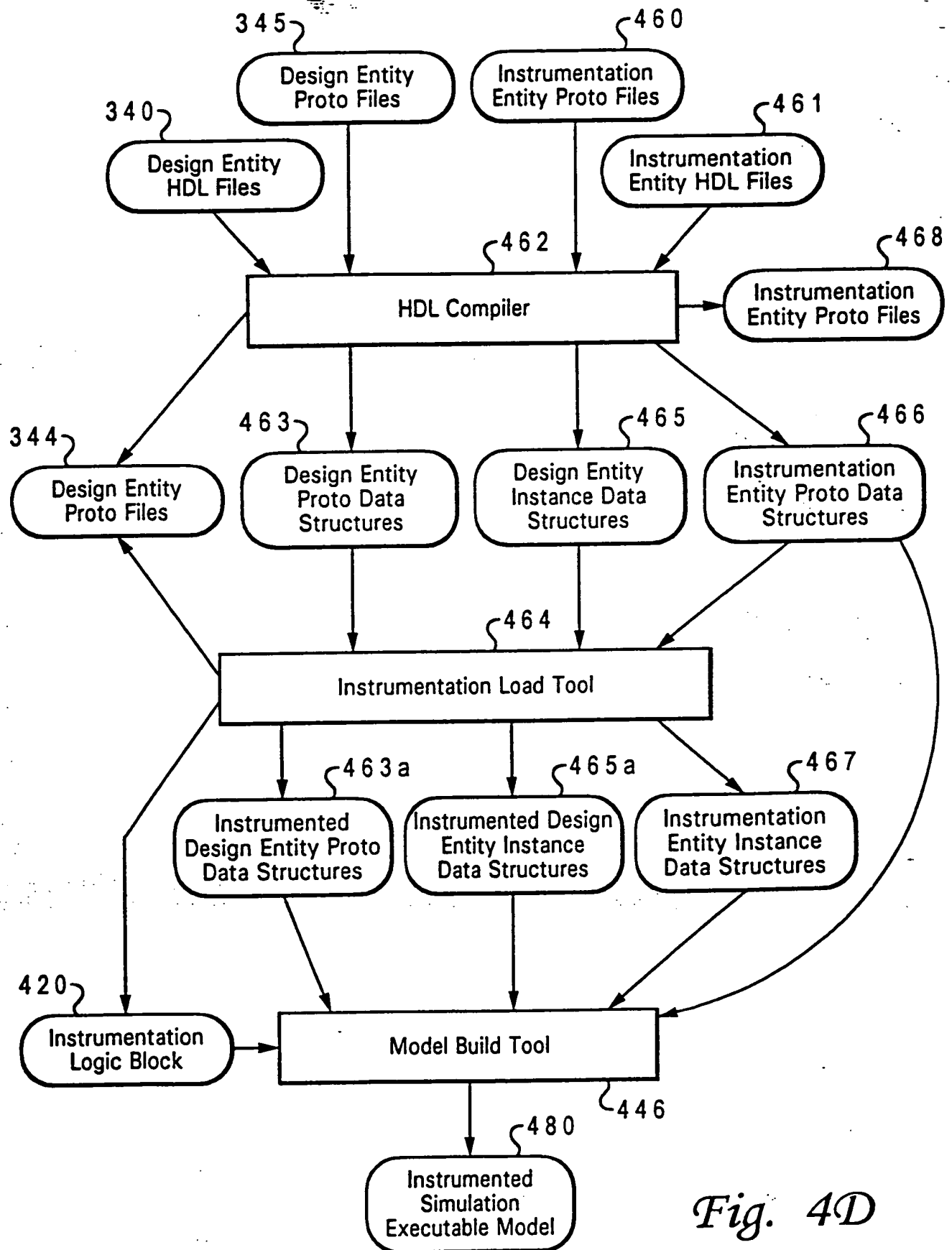
... HDL code for entity body section ...

END;

4 5 8

Fig. 4C

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*Fig. 4D*

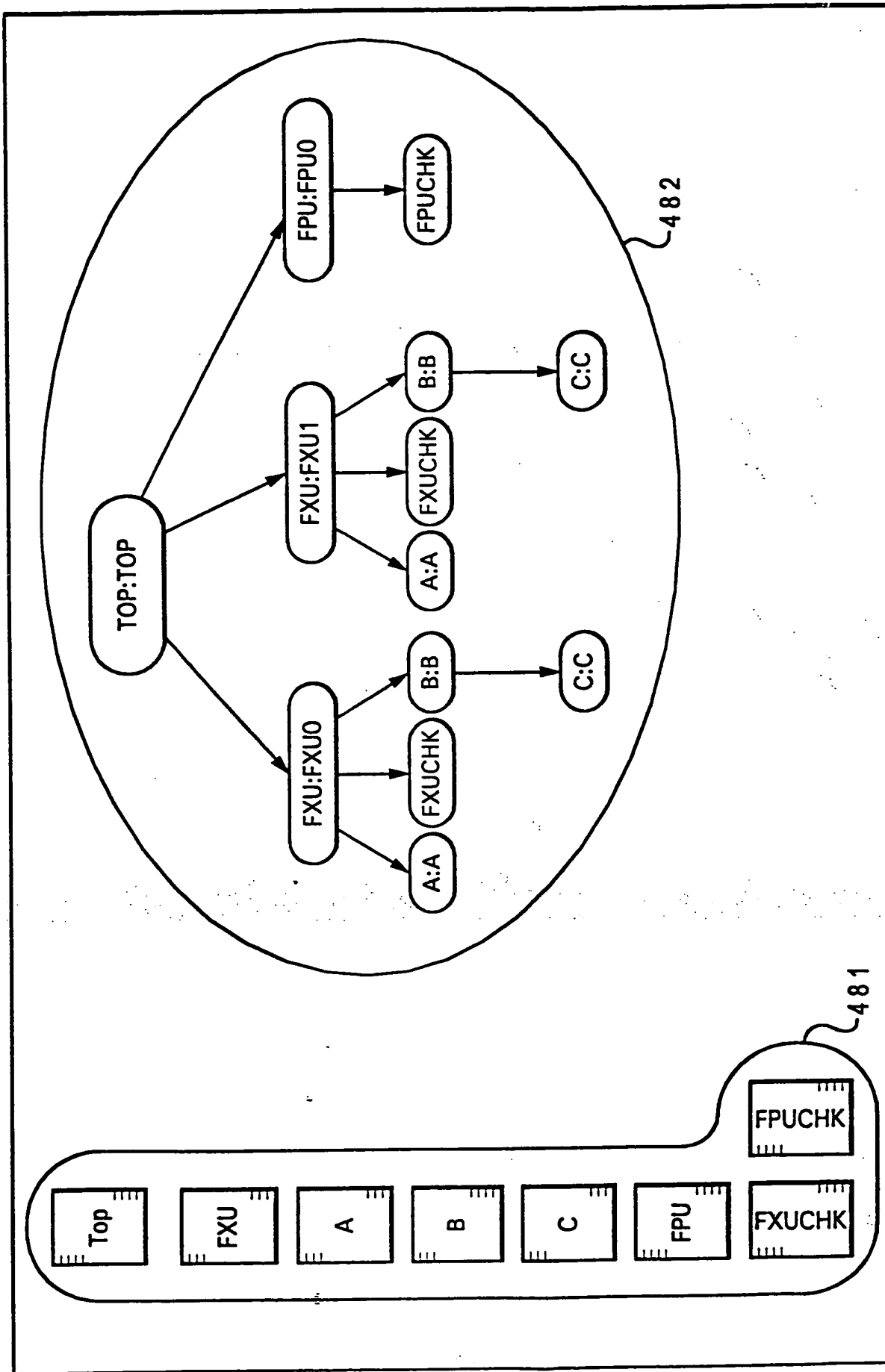


Fig. 4E





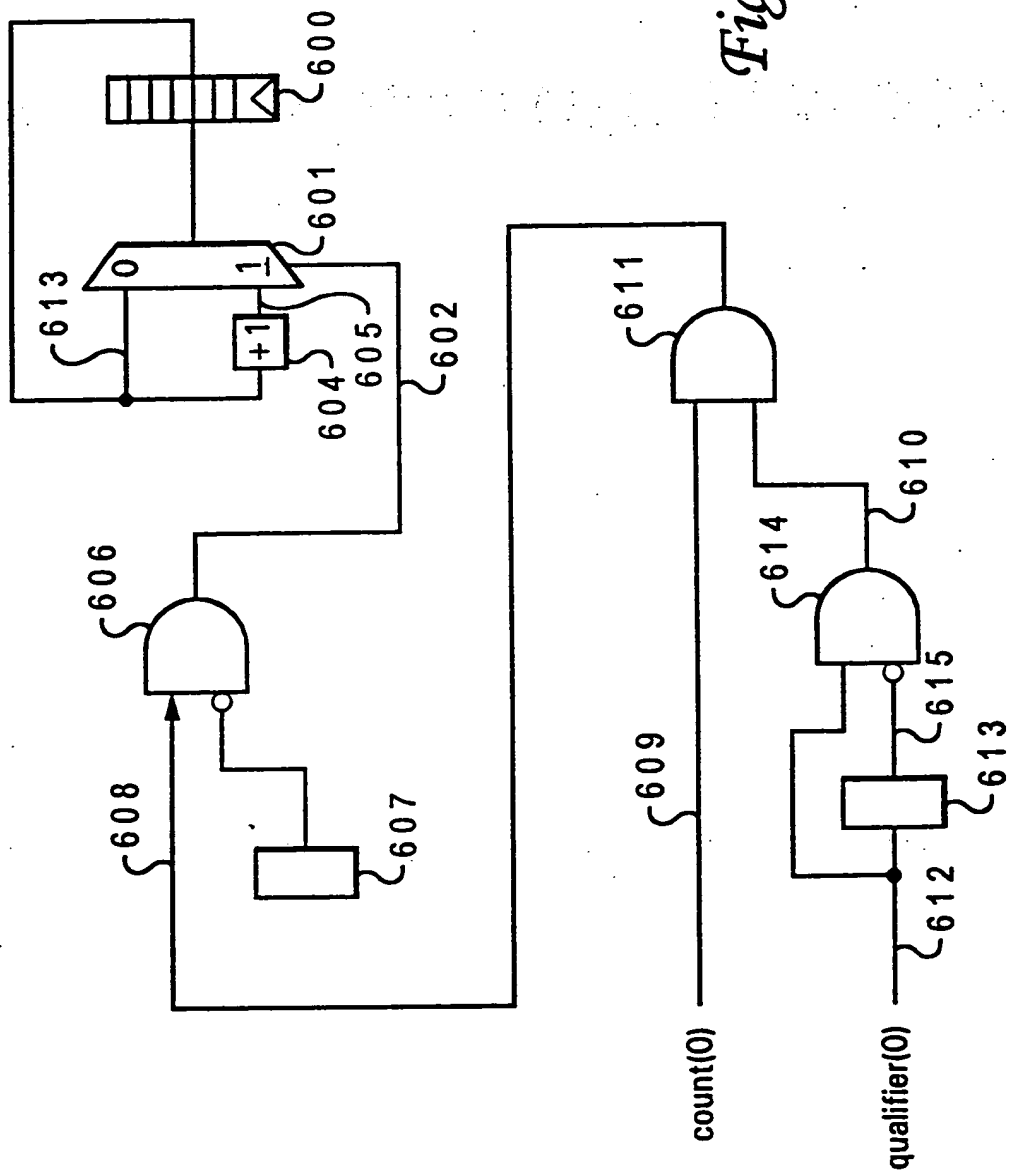


Fig. 6A

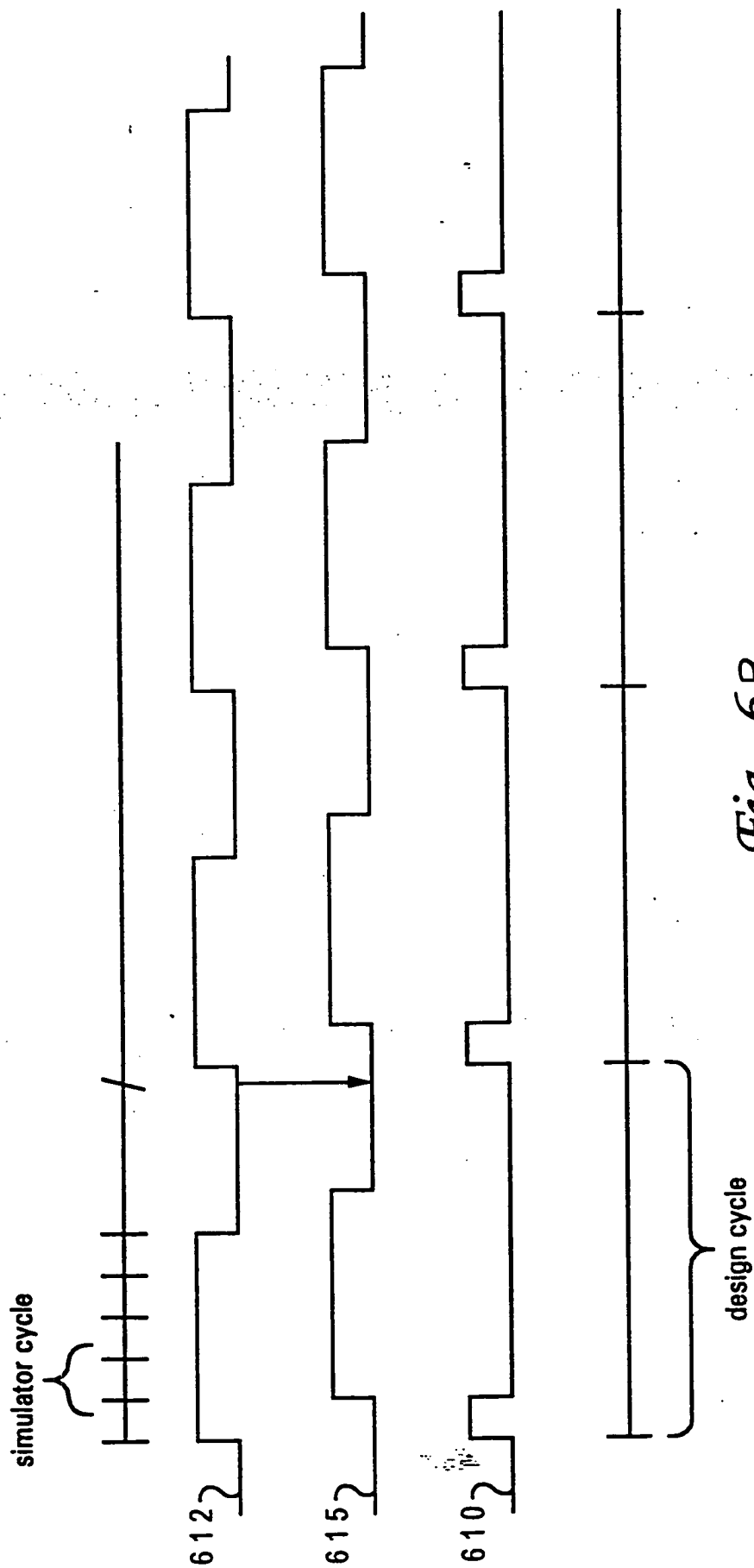


Fig. 6B

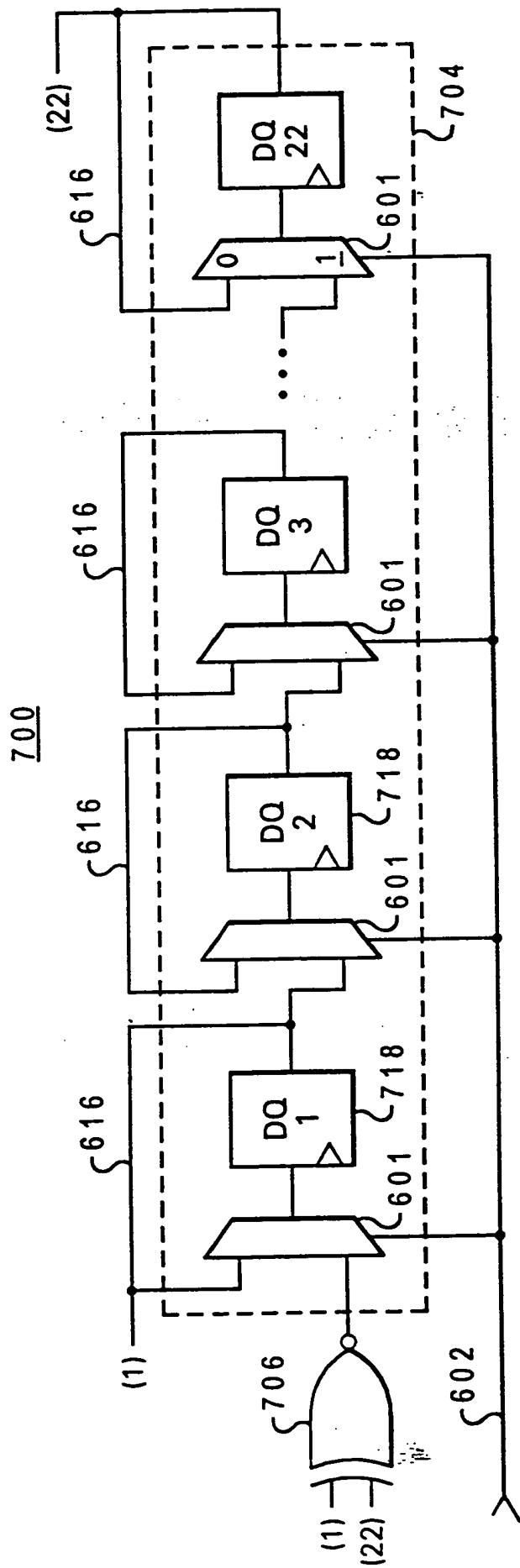


Fig. 7



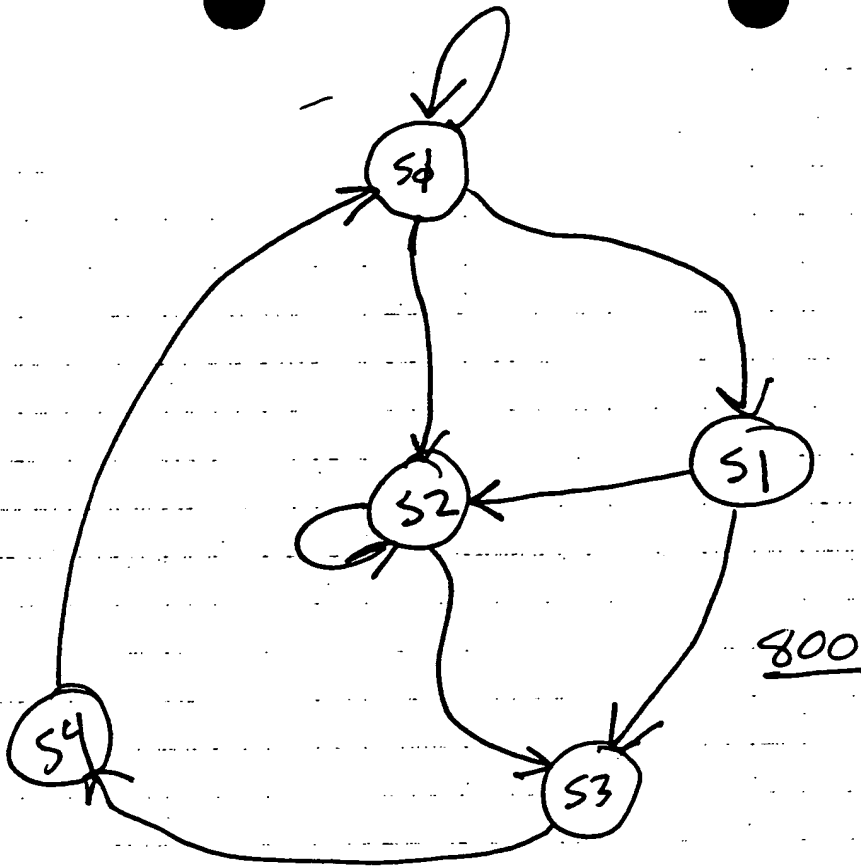


FIG. 8  
(Prior Art)

entity Fsm: Fsm

850

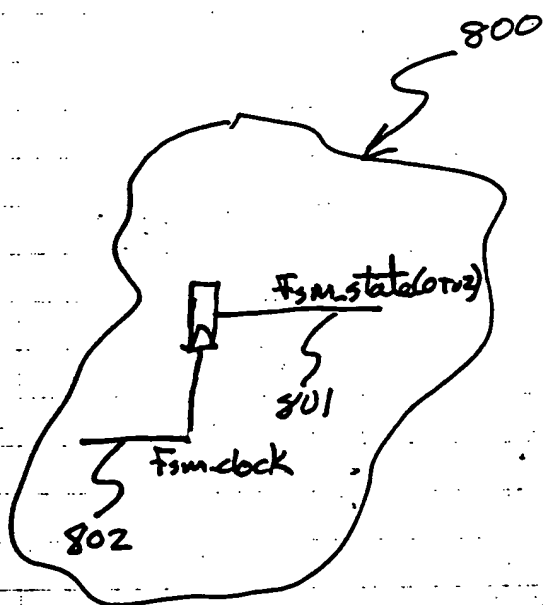


FIG. 8A  
(Prior Art)

entity Fsm IS

PORT (

.... ports for entity Fsm....

);

ARCHITECTURE Fsm of Fsm IS

BEGIN

.... HDL code for Fsm and rest of the entity...

fsm-state(0 to 2) <= ... signal 801....

```
853 E  --!! Embedded Fsm : exampleFsm;
859 E  --!! clock          : (fsm_clock);
854 E  --!! state-vector    : (fsm-state(0 to 2));
855 E  --!! states encoding : (s0, s1, s2, s3, s4);
856 E  --!! state-encoding  : ('000', '001', '010', '011', '100');
857 E  --!! arcs           : (s0 => s0, s0 => s1, s0 => s2,
                           s1 => s2, s1 => s3, s2 => s2,
                           s2 => s3, s3 => s4, s4 => s0);
858 E  --!! end Fsm;
```

852

86

END;

FIG. 8B

entity FSM:FSM

850

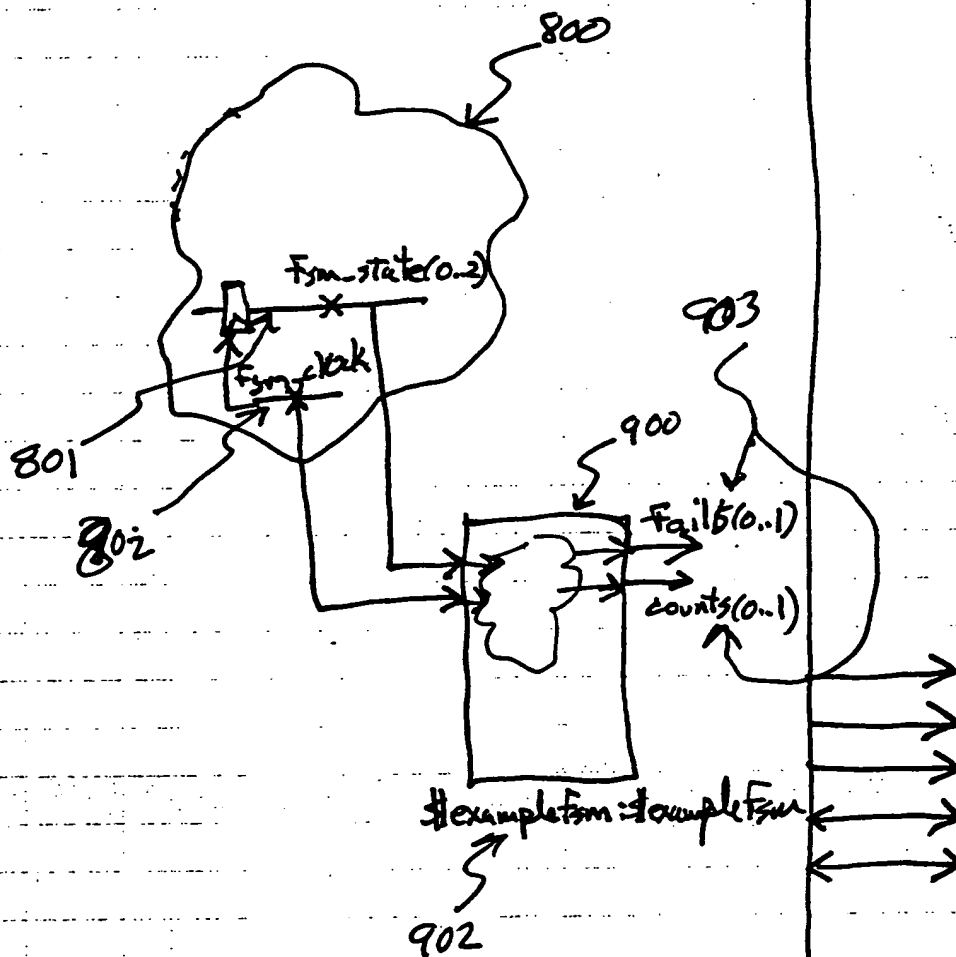
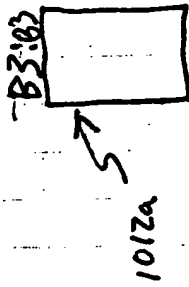


FIG. 9

TOP: TOP

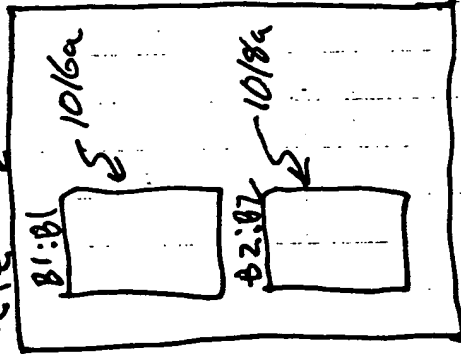
1010a

X: X1



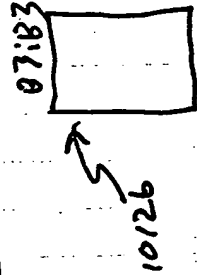
1014a

Z: Z



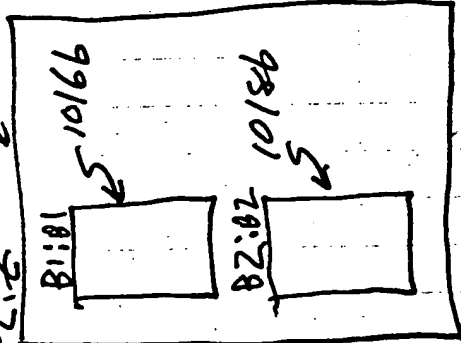
1010b

X: X2



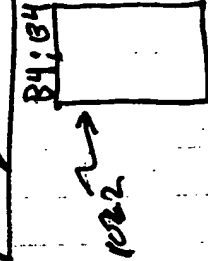
1014b

Z: Z



1010c

Y: Y



Z: Z

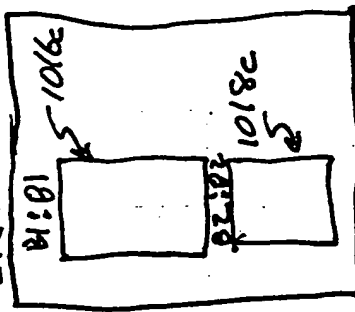


FIG. 10A

10303

10323

10343

10363

<instantiation identifier> . <instrumentation entity name> . <design entity name> . <event name>

FIG 10B

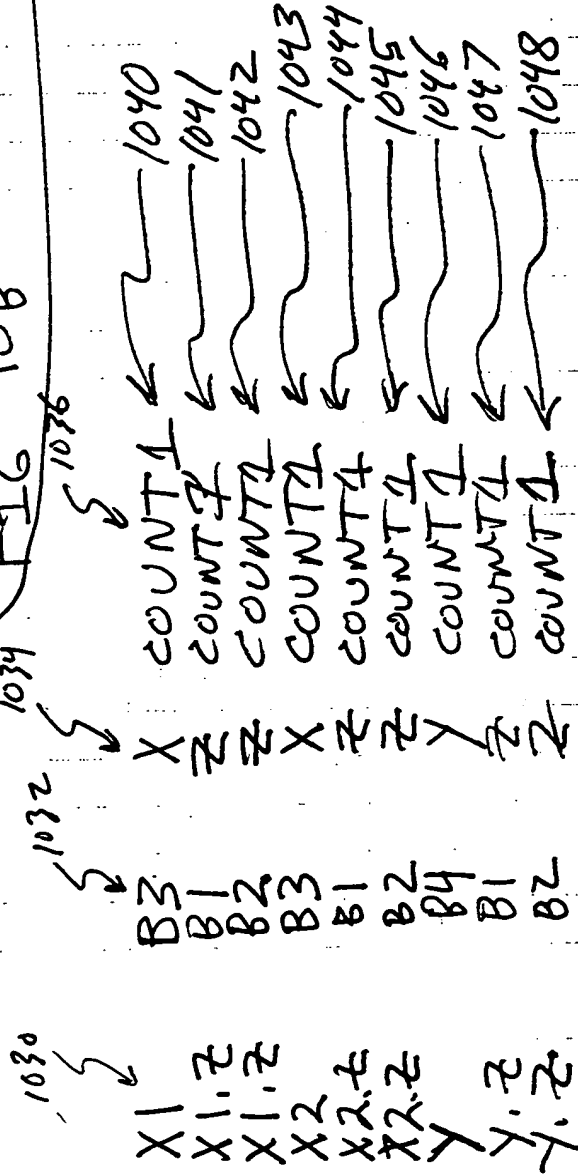


FIG 10C

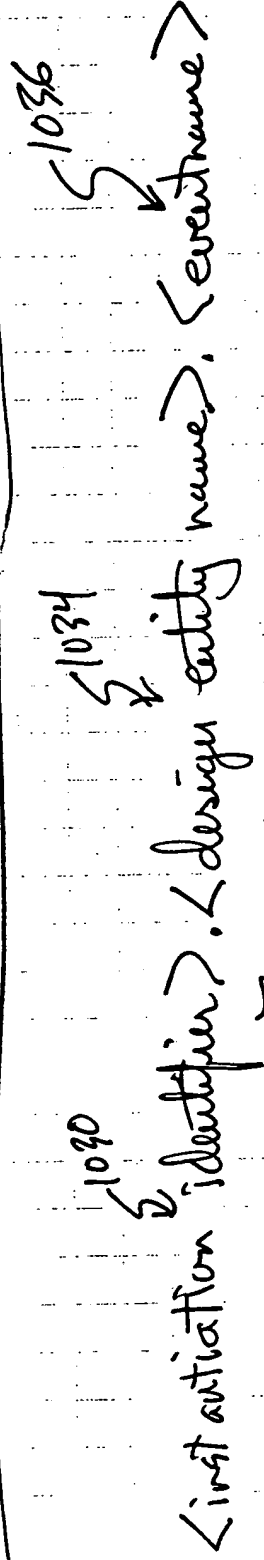


FIG. 10D

[illegible]

top: 104

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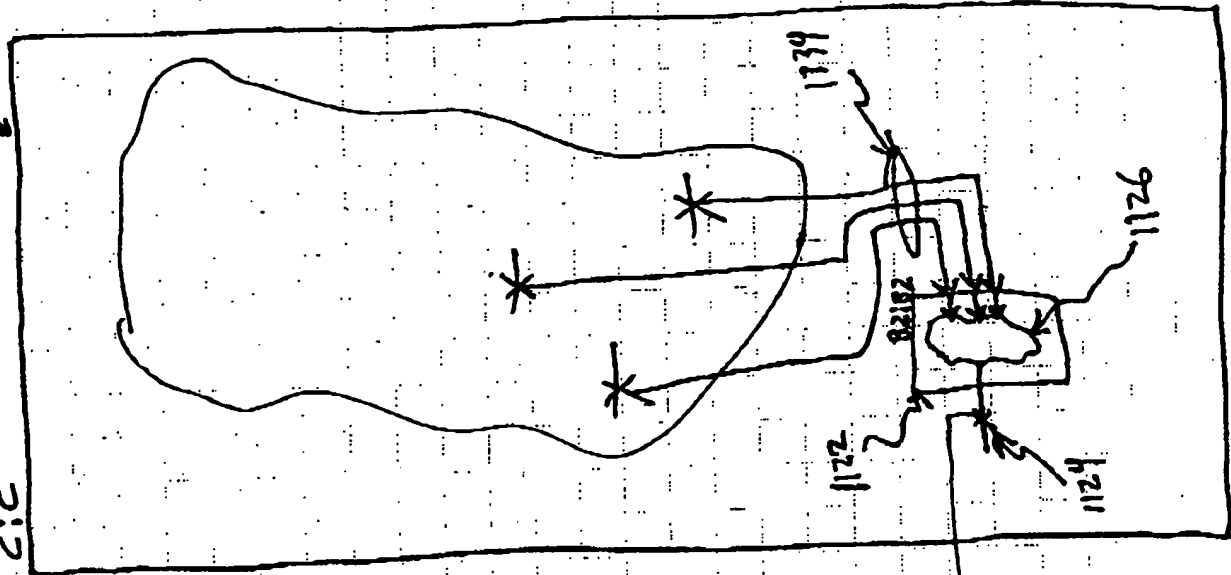
2011-5-1102

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**For:**

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1100

FIG. 11A

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--!! inputs 1165

--!! event\_1108\_in <= C.[B2.count.event\_1108]; 1161

--!! event\_1124\_in <= A.B.[B1.count.event\_1124]; 1162

--!! end inputs 1164 1166

FIG. 11B

--!! inputs

--!! event\_1108\_in <= C.[count.event\_1108]; 1171

--!! event\_1124\_in <= B.[count.event\_1124]; 1172

--!! end inputs

FIG. 11C



X:X

005231-0031550

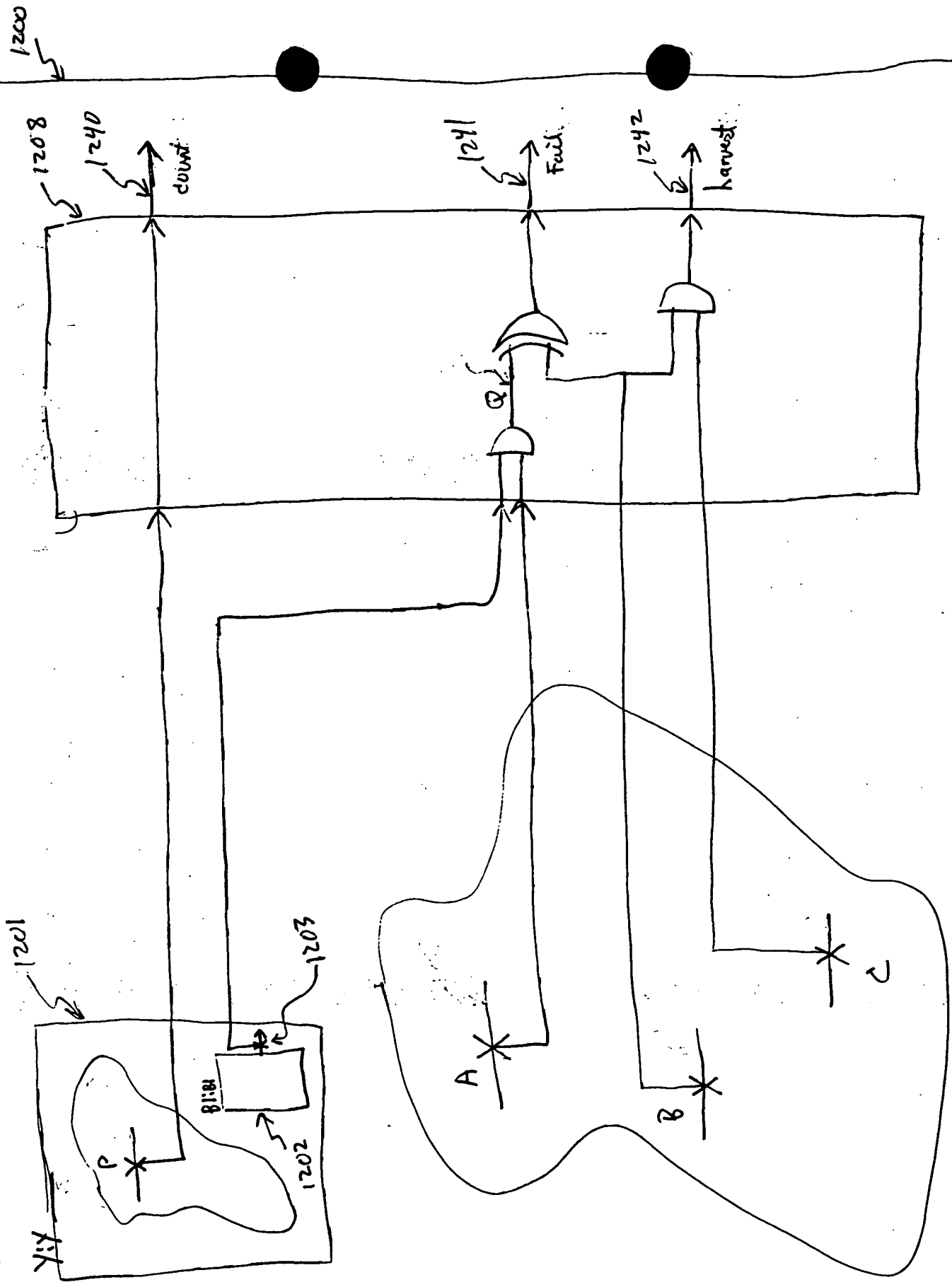


FIG. 12A

Entity X IS

PORT (  
;  
);

ARCHITECTURE example OF X IS

BEGIN

...HDL CODE FOR X....

Y:Y  
PORT MAP (  
);

1221

A <= ...  
B <= ...  
C <= ...

1222

--!! [count, countnameφ, clock] <= Y.P; } 1230  
--!! Q <= Y.[B].count.count1 AND A; } 1232  
--!! [fail, failnameφ, "fail msg"] <= Q XOR B; } 1234  
--!! [harvest, harvestnameφ, "harvest msg"] <= B AND C; } 1236 } 1223

END

FIG. 12B

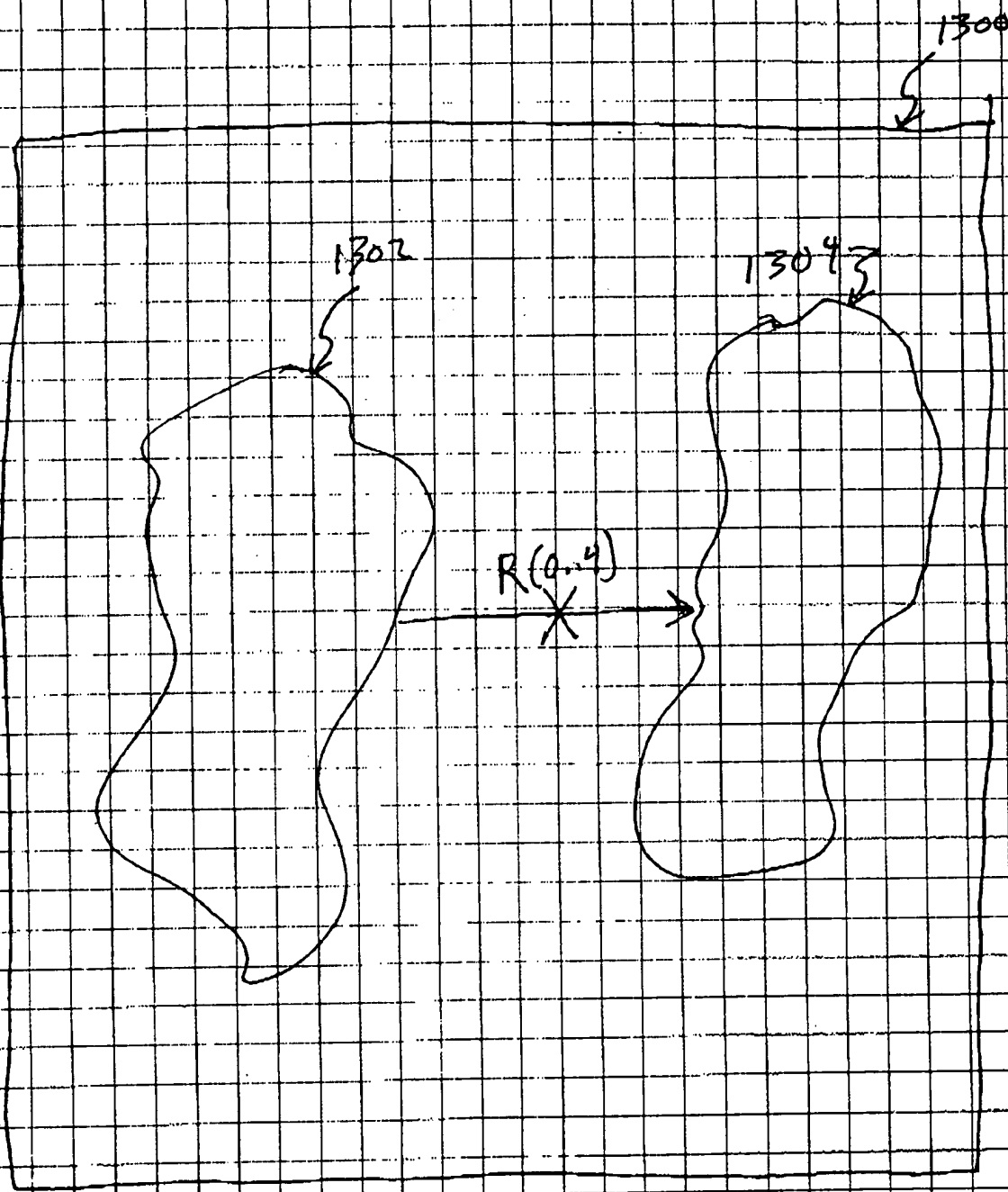
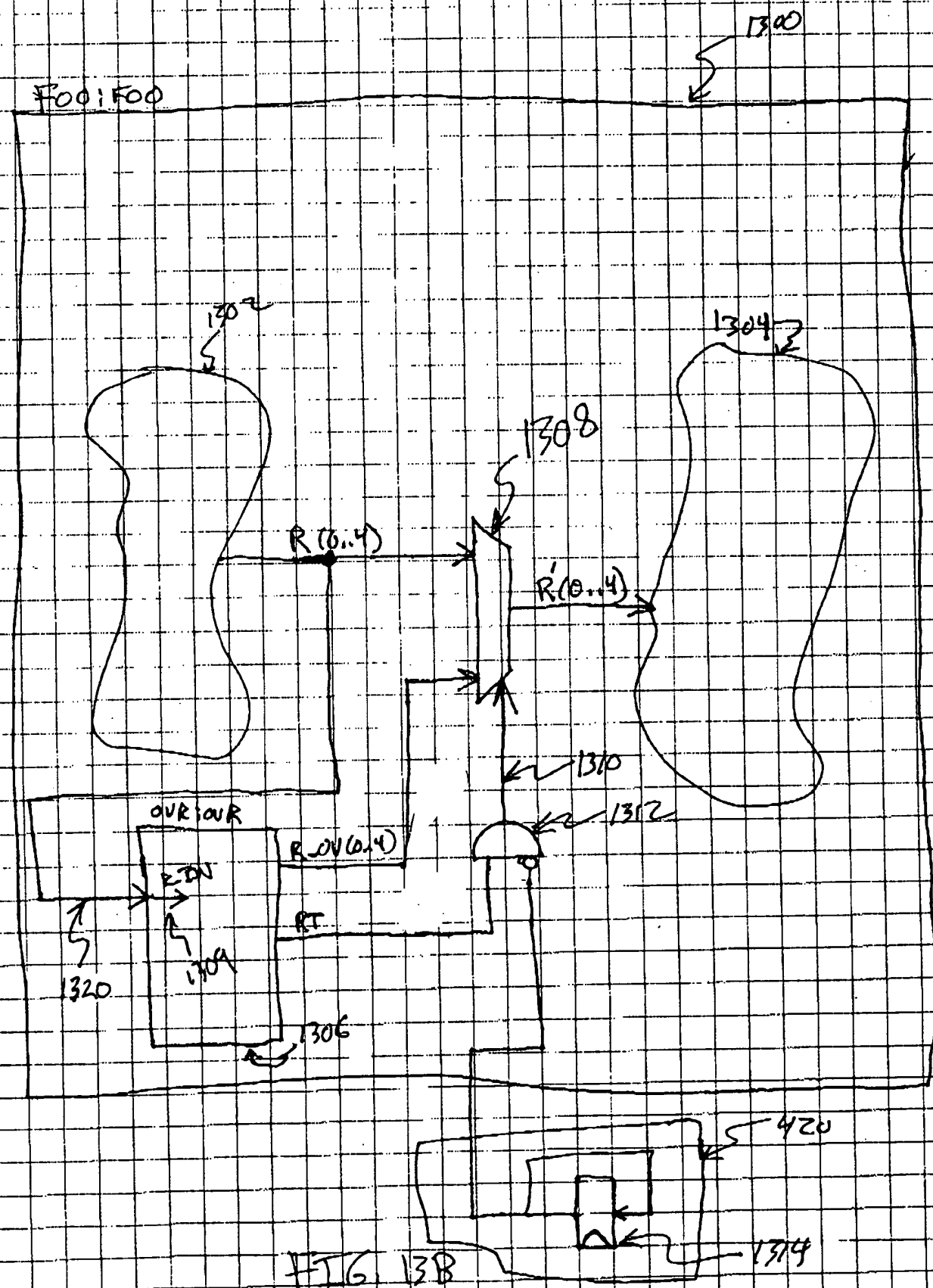


FIG. 13A



ENTITY OVR IS

PORT ( R\_IN : IN std\_logic\_vector(0..4);

-- other ports as required. --

R\_OV : OUT std\_logic\_vector(0..4);

RT : OUT std\_logic

);

-- !! BEGIN

-- !! Design Entity: FOO;

-- !! inputs (total)

-- !! R\_IN => R(0..4);

-- !! other ports as needed

-- !! END INPUTS

-- !! OUTPUTS

-- !! <R-OVERRIDE>: R\_OV(0..4) => R(0..4) [RT];

-- !! END OUTPUTS

-- !! END

ARCHITECTURE example of OVR IS

BEGIN

.... HDL code for entity body section. ....

END

FIG. 13C

ENTITY Foo IS

PORT (  
...  
);

ARCHITECTURE example of Foo IS

BEGIN

R <= ...

--!! R\_IN <= R;

--!! R\_OV(0..4) <= ...

--!! RT <= ...

--!! Override, R\_OVERRIDE, R(0..4), RT <= R\_OV(0..4);

384

FIG. 13D